

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	141	703/19.ccls.	USPAT	OR	OFF	2004/11/15 14:49
S2	0	703/19.ccls. and (local adj transformation)	USPAT	OR	OFF	2004/05/13 14:07
S3	28	(703/19.ccls. and delay) and reduction	USPAT	OR	OFF	2004/05/13 14:08
S4	118	703/19.ccls. and delay	USPAT	OR	OFF	2004/05/13 14:09
S5	54	(703/19.ccls. and delay) and (timing adj analysis)	USPAT	OR	OFF	2004/05/13 14:56
S6	5	703/19.ccls. and (timing adj optimization)	USPAT	OR	OFF	2004/05/13 15:00
S7	4754	(timing adj optimization)or (iterative adj refinement) or (logic adj resynthesis) or (timing adj resynthesis) or (synthesis adj techniques) or (logic adj optimization) or (delay adj reduction) or (local adj transformation)	USPAT	OR	OFF	2004/05/13 15:04
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S16	48	S15 and signal	USPAT	OR	OFF	2004/11/15 14:52
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S45	11	S44 and slack	USPAT	OR	OFF	2005/02/23 09:26
S46	0	S45 and fanin	USPAT	OR	OFF	2005/02/23 09:25

S47	1843	716/2,6.ccls.	US-PGPUB; USPAT	OR	OFF	2005/02/23 09:26
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S56	10	S55 and transformation	US-PGPUB; USPAT	OR	ON	2005/02/23 09:45
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✓ [Incremental techniques for the identification of statically sensitizable critical paths](#)

Yun-Cheng Ju, Resve A. Saleh

June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**Full text available: pdf(683.79 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

✓ [Session 10A: power analysis and optimization: Path selection and pattern generation for dynamic timing analysis considering power supply noise effects](#)

Jing Jia Liou, Angela Krstić, Yi Min Jiang, Kwang Ting Cheng

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**Full text available: pdf(73.10 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

Noise effects such as power supply and crosstalk can significantly affect the performance of deep submicron designs. These delay effects are highly input pattern dependent. Existing path selection and timing analysis techniques cannot capture the effects of noise on cell/interconnect delays. Therefore, the selected critical paths may not be the longest paths and predicted circuit performance might not reflect the worst-case circuit delay. In this paper, we propose a path selection technique that ...

✓ [Session 4C: delay budgeting and distribution: Potential slack: an effective metric of combinational circuit performance](#)

Chunhong Chen, Xiaojian Yang, Majid Sarrafzadeh

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**Full text available: pdf(55.96 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

This paper proposes the concept of potential slack and show it is an effective metric of combinational circuit performance. We provide several methods for estimating potential slack and prove one (a maximal-independent-set based algorithm) in particular works best. Experiments in gate sizing show that potential slack provides 100% correct prediction for circuit area optimization. We also explore the role of potential slack in timing-driven placement.

✓ [Sequential circuit delay optimization using global path delays](#)

Srimat T. Chakradhar, Sujit Dey, Miodrag Potkonjak, Steven G. Rothweiler

July 1993 **Proceedings of the 30th international conference on Design automation**

Full text available:  pdf(816.91 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

5 Speeding up technology-independent timing optimization by network partitioning

Rajat Aggarwal, Rajeev Murgai, Masahiro Fujita

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available:  pdf(189.22 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)


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Technology-independent timing optimization is an important problem in logic synthesis. Although many promising techniques have been proposed in the past, unfortunately they are quite slow and thus impractical for large networks. In this paper, we propose DEPART, a delay-based partitioner-cum-optimizer, which purports to solve this problem. Given a combinational logic network that is to be optimized for timing, DEPART divides it into sub-networks using timing information and a constraint on the m ...

6 Timing verification and the timing analysis program

R. B. Hitchcock

June 1988 **Papers on Twenty-five years of electronic design automation**

Full text available:  pdf(1.19 MB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

7 Exact required time analysis via false path detection

Yuji Kukimoto, Robert K. Brayton

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available:  pdf(133.77 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

 [Publisher Site](#)

This paper addresses how to compute required times at intermediate nodes in a combinational network given required times at primary outputs. The simplest approach is to compute them based on topological delay analysis without any consideration of false paths. In this paper, however, we take into account false paths between the intermediate nodes and the primary outputs explicitly to characterize the timing constraints at the nodes more accurately. We show that this approach leads to a technique for com ...

8 Transistor reordering for power minimization under delay constraint

S. C. Prasad, K. Roy

April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 1 Issue 2**

Full text available:  pdf(289.98 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this article we address the problem of optimization of VLSI circuits to minimize power consumption while meeting performance goals. We present a method of estimating power consumption of a basic or complex CMOS gate which takes the internal capacitances of the gate into account. This method is used to select an ordering of series-connected transistors found in CMOS gates to achieve lower power consumption. The method is very efficient when used by library-based design styles. We describe ...

Keywords: circuit optimization, critical path enumeration, gate input reordering, power estimation, transistor reordering

9 Hierarchical functional timing analysis

Yuji Kukimoto, Robert K. Brayton

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available:  pdf(239.20 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

 [Publisher Site](#)

We propose a hierarchical timing analysis technique for combinational circuits under the tightest known sensitization criterion, the XBDO delay model. Given a hierarchical combinational circuit, a generalized delay model of each left module is characterized first. Since this timing characterization step takes into account false paths in each module, the delay model is more accurate than the one obtained by topological analysis. Then topological delay analysis is performed on the circuit com ...

10 Design and optimization of low voltage high performance dual threshold CMOS circuits

Liqiong Wei, Zhanping Chen, Mark Johnson, Kaushik Roy, Vivek De

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available:  pdf(454.66 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

 [Publisher Site](#)

Reduction in leakage power has become an important concern in low voltage, low power and high performance applications. In this paper, we use dual threshold technique to reduce leakage power by assigning high threshold voltage to some transistors in non-critical paths, and using low-threshold transistors in critical paths. In order to achieve the best leakage power saving under target performance constraints, an algorithm is presented for selecting and assigning an optimal high threshold v_o ...

Keywords: MPEG4, codec, design automation, flip-flops, level converters, low power, placement, synthesis, voltage scaling

11 Timing Verification and the Timing Analysis program

Robert B. Hitchcock

January 1982 **Proceedings of the 19th conference on Design automation**

Full text available:  pdf(982.05 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Timing Verification consists of validating the path delays (primary input or storage element to primary output or storage element) to be sure they are not too long or too short and checking the clock pulses to be sure they are not too wide or too narrow. The programs addressing these problems neither produce input patterns like test pattern generators nor require input patterns like traditional simulators. Several programs (described here) operate by tracing paths [P173, WO78, SA81, ...

12 A deterministic approach to adjacency testing for delay faults

C. T. Glover, M. R. Mercer

June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation**

Full text available:  pdf(749.81 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Adjacency testing for delay faults is examined in both theory and implementation. We shall show that the necessary and sufficient conditions for adjacency testability yield an efficient method of robust delay test generation. Empirical results (including several different cost measurements) are presented which demonstrate that our technique: (1) achieves high fault coverages under both the robust and nonrobust delay fault models and (2) is cost effective.

13 Concurrent logic restructuring and placement for timing closure

Jinan Lou, Wei Chen, Massoud Pedram

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on**

Computer-aided designFull text available:  pdf(124.02 KB)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper, an algorithm for simultaneous logic restructuring and placement is presented. This algorithm first constructs a set of super-cells along the critical paths and then generates the set of non-inferior re-mapping solutions for each supercell. The best mapping and placement solutions for all super-cells are obtained by solving a generalized geometric programming (GGP) problem. The process of identifying and optimizing the critical paths is iterated until timing closure is achieved ...

14 Retiming-based factorization for sequential logic optimization

Surendra Bommur, Niall O'Neill, Maciej Ciesielski

July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3Full text available:  pdf(193.60 KB)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

Current sequential optimization techniques apply a variety of logic transformations that mainly target the combinational logic component of the circuit. Retiming is typically applied as a postprocessing step to the gate-level implementation obtained after technology mapping. This paper introduces a new sequential logic transformation which integrates retiming with logic transformations at the technology-independent level. This transformation is based on implicit retiming across logic blocks ...

Keywords: finite state machines, retiming, sequential synthesis**15 Wireplanning in logic synthesis**

Wilsin Gosti, Amit Narayan, Robert K. Brayton, Alberto L. Sangiovanni-Vincentelli

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**Full text available:  pdf(938.17 KB)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)**16 Low power synthesis of dual threshold voltage CMOS VLSI circuits**

Vijay Sundararajan, Keshab K. Parhi

August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design**Full text available:  pdf(751.10 KB)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)**17 Compression-relaxation: a new approach to performance driven placement for regular architectures**

Anmol Mathur, C. L. Liu

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**Full text available:  pdf(734.14 KB)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We present a new iterative algorithm for performance driven placement applicable to regular architectures such as FPGAs. Our algorithm has two phases in each iteration: a compression phase and a relaxation phase. We employ a novel compression strategy based on the longest path tree of a cone for improving the timing performance of a given placement. Compression might cause a feasible placement to become infeasible. The concept of a slack neighborhood graph is introduced and is used in the r ...

18**Optimization of critical paths in circuits with level-sensitive latches**

Timothy M. Burks, Karem A. Sakallah

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**


Full text available:  pdf(652.85 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

A simple extension of the critical path method is presented which allows more accurate optimization of circuits with level-sensitive latches. The extended formulation provides a sufficient set of constraints to ensure that, when all slacks are non-negative, the corresponding circuit will be free of late signal timing problems. Cycle stealing is directly permitted by the formulation. However, moderate restrictions may be necessary to ensure that the timing constraint graph is acyclic. Forcin ...

19 Fast module mapping and placement for datapaths in FPGAs

Timothy J. Callahan, Philip Chong, André DeHon, John Wawrzynek

March 1998 **Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays**

Full text available:  pdf(1.26 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

By tailoring a compiler tree-parsing tool for datapath module mapping, we produce good quality results for datapath synthesis in very fast run time. Rather than flattening the design to gates, we preserve the datapath structure; this allows exploitation of specialized datapath features in FPGAs, retains regularity, and also results in a smaller problem size. To further achieve high mapping speed, we formulate the problem as tree covering and solve it efficiently with a linear-time dynamic pr ...

20 Area and delay mapping for table-look-up based field programmable gate arrays

P. Sawkar, D. Thomas

July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**

Full text available:  pdf(571.21 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

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☒ 1 Delay-fault diagnosis by critical-path tracing

Girard, P.; Landrault, C.; Pravossoudovitch, S.;
 Design & Test of Computers, IEEE , Volume: 9 , Issue: 4 , Dec. 1992
 Pages:27 - 32

[\[Abstract\]](#) [\[PDF Full-Text \(700 KB\)\]](#) IEEE JNL

☒ 2 Hierarchical test generation and design for testability methods for ASPPs and ASIPs

Ghosh, I.; Raghunathan, A.; Jha, N.K.;
 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 , Issue: 3 , March 1999
 Pages:357 - 370

[\[Abstract\]](#) [\[PDF Full-Text \(368 KB\)\]](#) IEEE JNL

☒ 3 A design-for-testability technique for register-transfer level circuits using control/data flow extraction

Ghosh, I.; Raghunathan, A.; Jha, N.K.;
 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 , Issue: 8 , Aug. 1998
 Pages:706 - 723

[\[Abstract\]](#) [\[PDF Full-Text \(360 KB\)\]](#) IEEE JNL

☒ 4 An algorithm for test generation of combinational circuits research and implementation for critical path tracing

Yin, S.; Wei, D.-Z.;
 Test Symposium, 1993., Proceedings of the Second Asian , 16-18 Nov. 1993
 Pages:26 - 30

[\[Abstract\]](#) [\[PDF Full-Text \(448 KB\)\]](#) IEEE CNF

5 **Delay-fault diagnosis based on critical path tracing from symbolic simulation**

Girard, P.; Landrault, C.; Pravossoudovitch, S.;

Circuits and Systems, 1992. ISCAS '92. Proceedings., 1992 IEEE International Symposium on , Volume: 3 , 3-6 May 1992

Pages:1133 - 1136 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(336 KB\)\]](#) [IEEE CNF](#)

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